## REMARKS

Rejection of claims 1-10 and 14-30 is maintained under 35 U.S.C. §103(a) over Liu et al., U.S. Patent No. 6,345,072B1 (hereinafter "Liu"). Likewise, claims 11-13 stand rejected further in view of Cheng et al., U.S. Patent No. 6,456,650B1 (hereinafter "Cheng"), as being obvious.

Claim 1 calls for an asymmetric digital subscriber loop (ADSL) modem including an integrated circuit that may contain an analog-to-digital converter to produce data at a relatively higher data rate. In the integrated circuit, a *device may couple to the analog-to-digital converter to reduce the higher data rate data from the analog-to-digital converter to a lower data rate.* Finally, a multiplexer may *multiplex the lower data rate data and control information and transmit* the data and control information *externally of the integrated circuit.*

Even though the Examiner maintains rejection of all claims as stated in the previous Office Action, the Applicants respectfully submit that a different limitation may resolve the rejections indicated above. In the § 103 rejection of claim 1, the Examiner contends that the prior art voice band modem implementation shown in Figure 1A and 1B of the Liu reference discloses the claimed ADSL modem within which multiplexed data is transmitted external of the integrated circuit when the data is at a reduced or lower data rate. However, data transmitted between the voice band modem digital circuitry 130 and the voice band analog circuitry 110 is at a relatively higher data rate, resulting in more buffering at each circuitry. As a result, a *prima facie* case of obviousness is not made out.

Specifically, the voice band analog circuitry 110 transmits the data at a rate based on the high clocking rate of the serial clock. That is, instead of transmitting the data when the data is at a reduced or lower data rate, which results in decreased cost, the voice band analog circuitry 110 simply transmits data at a relatively higher data rate. Thus, there is no indication of a device that may reduce the higher data rate data from an analog-to-digital converter to a lower data rate for a multiplexer to transmit the multiplexed lower data rate data and control information out of an integrated circuit in which the device and the multiplexer are located for an asymmetric digital subscriber loop modem, as claimed in claim 1.

Specifically, in Figure 1A, the prior art voice band modem implementation merely discloses two serial, time division multiplexed input/output data streams to and from the PC, i.e., SDATA_OUT, and SDATA_IN, respectively. An audio modem codec utilizes a single receive

data line (SDATA_OUT) and a single transmit data line (SDATA_IN). This *single line approach requires a high clocking rate which does not permit xDSL type modem implementation* that requires a much higher bit rate than possible from even a high clocking rate such as 12.288 megahertz (MHz). See column 2, lines 48-55 and column 8, lines 24-30 in the Liu reference.

The Examiner states that the Liu reference suggests that digital filters will be used for the purposes of interpolation and decimation on either side of the DSL link with four receive (Rx1 – Rx4) and four transmit (Tx1 – Tx4) data lines in the xDSL modem 200 shown in Figures 2A and 2B when oversampling is used in A/D and D/A converters 213, 213'. As such, a digital filter commonly uses a processor, such as a DSP to perform numerical calculations on sampled values of the signal which is represented by a sequence of numbers, rather than a voltage or current in the analog form. In oversampling architecture based A/D and D/A converters, while the interpolation filter is used within a typical delta-sigma A/D converter itself, the decimation filter is an integral part of a typical sigma-delta D/A converter.

However, an interpolation filter within a typical sigma-delta D/A converter brings the input sample rate up to the modulation rate. Instead, a decimation filter is used within a typical delta-sigma modulator, which has a high sampling rate, to generate the digital output of the delta-sigma A/D converter at the desired frequency. In view of this, characterizations of the digital filters 214 and 214' as interpolation and decimation filters, respectively, where use of oversampled A/D and D/A converters is also intended, are inconsistent with otherwise known usage of a digital filter.

Therefore, absent the benefit of the Applicant's specification, the cited reference fails to convey or suggest use of a device coupled to an analog-to-digital converter to reduce the higher data rate data from the analog-to-digital converter to a lower data rate as set forth above because hindsight reconstruction is improper. Even worse, the mere fact that the cited reference may be modified in the manner suggested by the Examiner does not make the modification obvious unless the cited reference suggested the desirability of the modification, transmitting multiplexed data at a lower data rate external of the integrated circuit within the ADSL modem of claim 1. Therefore, obviousness cannot be established based on the teachings or suggestions set forth above to produce the claimed invention in claim 1.

Thus, Liu neither teaches nor suggests use of a device coupled to an analog-to-digital converter to reduce the higher data rate data from the analog-to-digital converter to a lower data rate. Absent a specific teaching or suggestion to use a multiplexer that multiplexes the lower data rate data and control information for transmission external of the integrated circuit and the device to implement the ADSL modem of claim 1, for this reason alone, Liu fails to disclose all limitations of claim 1. Dependent claims on claim 1 are patentable for at least the reason that these claims depend from an allowable claim. For similar reasons, other rejected independent claims and the remaining dependent claims are likewise in condition for allowance. The Examiner is respectfully requested to reconsider all pending claims.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

Date: April 30, 2003

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Attorney Docket No. :ITL.0296US (P6509) TNT/SKS:dlc

Applicants: MICHAEL J. MCTAGUE, ET AL.
Serial No.: 09/471,435
Filing Date: December 23, 1999
Title: ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

1. Reply to Paper No. 8;
2. Limited Recognition to Prosecute Patent Application; and
3. Fax Coversheet.